AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A cache memory employing a set associative system, for generating a valid bit for showing presence of validity of a cache data, comprising:

a storage for storing an address tag of an address of a cache data and a first valid bit for showing presence of validity of said cache data in a set of blocks in response to an index; and

reset means for storing a second valid bit corresponding to said first valid bit, and resetting said second valid bit,

wherein said valid bit is generated based on the first valid bit and the second valid bit.

2. (Currently Amended) A cache memory recited in claim 1, ~~characterized in that~~ wherein said valid bit shows validity in case that both of the first valid bit and the second valid bit show validity, and shows invalidity in case that either the first valid bit or the second valid bit shows invalidity.

3. (Original) A cache memory recited in claim 1, wherein said reset means is common to each way.

4. (Currently Amended) A cache memory recited in claim 1, ~~characterized in that~~ wherein, in case that said reset means resets the second valid bit, said first valid bit is cleared via write means for writing the first valid bit into the storage.

5. (Original) A cache memory recited in claim 4, wherein said first valid bit is selectively cleared via the write means.

6. (Currently Amended) A control method of controlling a reset of a cache memory employing a set associative system, for generating a valid bit for showing presence of validity of a cache data, comprising ~~the steps of~~:

storing an address tag of an address of a cache data and a first valid bit for showing presence of validity of said cache data in a set of blocks in response to an index;

storing a second valid bit in response to said index;

resetting said second valid bit; and

generating said valid bit based on said first valid bit and said second valid bit.

7. (Currently Amended) A control method recited in claim 6, ~~characterized in that~~ wherein said valid bit shows validity in case that both of the first valid bit and the second valid bit show validity, and shows invalidity in case that either the first valid bit or the second valid bit shows invalidity.

8. (Currently Amended) A control method recited in claim 6, ~~characterized in that~~ wherein, in case that the second valid bit is reset, the address tag and the first valid bit are stored and said first valid bit is cleared.

9. (Original) A control method recited in claim 8, wherein said first valid bit is selectively cleared.

Please add new claims as follows:

10. (New) A cache memory employing a set associative system, for generating a valid bit for showing presence of validity of a cache data, comprising:

a storage that stores an address tag of an address of a cache data and a first valid bit that shows presence of validity of said cache data in a set of blocks in response to an index; and

a reset unit that stores a second valid bit corresponding to said first valid bit, and resets said second valid bit,

wherein said valid bit is generated based on the first valid bit and the second valid bit.

11. (New) A cache memory recited in claim 10, wherein said valid bit shows validity in case that both of the first valid bit and the second valid bit show validity, and shows invalidity in case that either the first valid bit or the second valid bit shows invalidity.

12. (New) A cache memory recited in claim 10, wherein said reset unit is common to each way.

13. (New) A cache memory recited in claim 10, wherein, in case that said reset unit resets the second valid bit, said first valid bit is cleared via a write unit that writes the first valid bit into the storage.

14. (New) A cache memory recited in claim 13, wherein said first valid bit is selectively cleared via the write unit.